

## **DETAILED ACTION**

### ***Status of the Claims***

1. Amendment filed May 3, 2007 is acknowledged. Claim 6 has been cancelled. Claims 1, 5 and 13 have been amended. Claims 1-5, 7-10 and 13-18 are pending.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-5, 7-10 and 13-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation “wherein the Schottky consumes 2.5-**4.5** % of the active area” (claims 1 and 13) in the application as filed.

The specification fails to provide support for the actual value of “2.5-**4.5** %”.

As can be seen through out the disclosure, there are many percentage area of the Schottky structure disclosed, i.e., 2.5%, 5%. However, the specific range of 2.5% to **4.5**% was not once addressed. Although the value of 4.5% is within the range of 2.5% to 5%, the value of **4.5**% does not exist 4.5% until the value of 5% were rejected on merits.

Applicant must cancel the new matter.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-5, 7 and 8 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp (U.S. Patent No. 6,351,018) in view of Korman et al. (U.S. Patent No. 5,111,253) both of record.

With respect to claim 1, as best understood by the examiner, Sapp teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure (306) in an active area of a semiconductor substrate substantially as claimed, wherein:

the field effect transistor comprises:

a first trench (300-1) extending into the substrate and including a conductive material (302) forming a gate electrode of the field effect transistor; and

a pair of doped source regions (n<sup>+</sup>) positioned adjacent to and on opposite sides of the trench (300-1) and inside a doped body region, the doped source regions (n<sup>+</sup>) forming a source electrode of the field effect transistor, and the substrate forming a drain electrode of the field effect transistor, and

the Schottky structure (210) comprises:

a pair of adjacent trenches (300-3; 300-4) extending into the substrate, the pair of adjacent trenches (300-3; 300-4) including a conductive material (302) which is separated from trench side-walls by a thin layer of dielectric; and

a Schottky diode having a barrier layer formed on the surface of the substrate and between the pair of adjacent trenches (300-3; 300-4);

wherein the Schottky structure consumes a portion of the active area, and the field effect transistor consumes the remaining portion of the active area. (See Figs. 2-7).

Thus, Sapp is shown to teach all the features of the claim with the exception of explicitly disclosing a specific percentage of area occupied by the Schottky structure.

Sapp further teaches: since the area of the Schottky diode determines its forward voltage drop in response to current, Schottky structures with different numbers of adjacent trenches can *be devised to arrive at the desired area*. (See col. 5, lines 3-6, emphasis added).

However, Korman teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure in an active area of a semiconductor substrate, the Schottky diode occupies between about 5% (approximate 4.5%) to about 50% of the active area. Korman further teaches: “The specific percentage which is optimum depends on the expected diode current density, the turn-on voltage of the Schottky diode and the thickness and resistivity of the drift region. *The optimum value can be easily determined experimentally.*” (See col. 8, lines 17-32).

Note that the specification contains no disclosure of either the critical nature of the *claimed Schottky structure consumes 2.5% to 4.5% of active area* or of any unexpected results arising therefrom. Where patentability is aided or based upon a particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the monolithically integrated structure of Sapp having an optimized active area consumes by the Schottky structure, as low as about 5%, as taught by Korman to enhance the performance characteristic of the MOSFET switch, since such a modification would have involved a mere optimization, experimentally, of the total area consumed by the Schottky diode of Sapp, in view of Korman.

Additionally, within purview of one having ordinary skill in the art, guided by the teaching of Sapp and Korman, particularly, it would have been obvious to determine the optimum area occupied by the Schottky diode. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) “It is not inventive to discover optimum or workable ranges by routine experimentation”.

Further, Applicant clearly admitted that “a ratio of the total area of the Schottky structure to the total area of the MOSFET in the range of 2.5% to 5% results in optimum performance”. (See page 6, lines 24-26).

With respect to claim 2, the field effect transistor of Sapp further comprises a metal layer contacting the pair of doped source regions (n+), the metal layer and the barrier layer comprise one of either titanium tungsten or titanium nitride.

With respect to claim 3, the barrier layer and the metal layer of Sapp contacting the source regions (n+) connect together by an overlying layer of metal. (See Fig. 3).

With respect to claim 4, the barrier layer of Sapp forms the Schottky diode anode (304) terminal and the substrate forms the Schottky diode cathode terminal.

With respect to claim 5, the integrated structure of Sapp further comprises a second trench (300-2) adjacent to the first trench (300-1), the second trench (300-2) including a conductive material (302), wherein a distance between the first trench (300-1) and the second trench (300-2) is greater than a distance W separating the pair of adjacent trenches (300-3; 300-4), and wherein the barrier layer and a metal layer contacting the source regions (n+) of the field effect transistor comprise one of either titanium tungsten or titanium nitride.

With respect to claim 7, the conductive material of Sapp in the pair of adjacent trenches (300-3; 300-4) between which the Schottky diode is formed is electrically isolated from the conductive material (302-1) in the first trench (300-1).

With respect to claim 8, the conductive material of Sapp in the pair of adjacent trenches between which the Schottky diode is formed, is recessed into the pair of adjacent trenches and covered by a layer of dielectric material. (See Fig. 4).

4. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp '018 and Korman '253 as applied to claim 1 above, and further in view of Hurst et al. (U.S. Patent No. 6,437,386) of record.

Sapp teaches a monolithically integrated structure as described in claim 1 above including a first trench (300-1) extending into the substrate, wherein an insulating layer formed lining the side and bottom of the first trench.

Thus, Sapp is shown to teach all the features of the claim with the exception of the thickness of the insulating layer of the first trench as well as the pair of adjacent trenches along the bottom is thicker than that along the sidewalls.

However, Hurst teaches dielectric layer formed along the bottom (27) of a trench is thicker than that formed along the sidewalls (21) substantially reduces gate charge to reduce gate-to-drain capacitance thereby increasing the efficiency and prolong the life of the semiconductor device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the insulating layer lining the trenches of Sapp thicker on the bottom than on the sidewalls as taught by Hurst to reduce gate-to-drain capacitance thereby increasing the efficiency and prolong the life of the semiconductor device.

5. Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp '018 in view of Baliga (U.S. Patent No. 5,998,833) and Korman '253, all of record.

With respect to claim 13, as best understood by the examiner, Sapp teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure (210) in an active area of a semiconductor substrate (202) substantially as claimed, wherein:

the field effect transistor comprises:

a first trench (200-2) extending into the substrate;

a second conductive material (206) forming a gate electrode in the first trench (200-1);

a pair of doped source regions (212) positioned adjacent to and on opposite sides of the first trench (200-2) and inside a doped body region (214), the doped source regions (212) forming a source electrode of the field effect transistor, and the substrate forming a drain electrode of the field effect transistor, and

the Schottky structure (210) comprises:

a pair of adjacent trenches (200-3; 200-4) extending into the substrate (202), each pair of adjacent trenches (200-3; 300-4) including a conductive material (206); and

a Schottky diode (210) having a barrier layer (218) formed on the surface of the substrate (202) and between the pair of adjacent trenches (300-3; 300-4);

wherein the Schottky structure (210) consumes a portion of the active area, and the field effect transistor consumes the remaining portion of the active area. (See Figs. 2).

Thus, Sapp is shown to teach all the features of the claim with the exception of explicitly disclosing a first conductive material forming a shield electrode formed in the bottom and separated from the second, upper conductive material and a specific percentage of area occupied by the Schottky structure.

However, Baliga teaches the field effect transistor can be alternatively made including:

a first trench (20) extending into the substrate (10);

a first conductive material (26) forming a shield electrode in the bottom portion of the trench (20);

a second conductive material (30) forming a gate electrode in the trench (20), the second conductive material (30) being over but insulated from the first conductive material (26). (See Fig. 4H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the field effect transistor of Sapp including two separate conductive materials filling the trench as taught by Baliga to reduce the gate-to-drain capacitance and improve switching speed.

With respect to claim to the specific area occupied by the Schottky structure, Sapp further teaches: since the area of the Schottky diode determines its forward voltage drop in response to current, Schottky structures with different numbers of adjacent trenches *can be devised to arrive at the desired area*. (See col. 5, lines 3-6, emphasis added).

However, Korman teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure in an active area of a semiconductor substrate, the Schottky diode occupies between about 5% (approximate 4.5%) to about 50% of the active area. Korman further teaches: “The specific percentage which is optimum depends on the expected diode current density, the turn-on voltage of the Schottky diode and the thickness and resistivity of the drift region. *The optimum value can be easily determined experimentally.*” (See col. 8, lines 17-32).

Note that the specification contains no disclosure of either the *critical nature of the claimed Schottky structure consumes 2.5% to 4.5% of active area* of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the monolithically integrated structure of Sapp having an optimized active area consumes by the Schottky structure, as low as about 5%, as taught by Korman to enhance the performance characteristic of the MOSFET switch, since such a modification would have involved a mere optimization, experimentally, of the total area consumed by the Schottky diode of Sapp, in view of Korman.

Additionally, within purview of one having ordinary skill in the art, guided by the teaching of Sapp and Korman, particularly, it would have been obvious to determine the optimum area occupied by the Schottky diode. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) “It is not inventive to discover optimum or workable ranges by routine experimentation”.

Further, Applicant clearly admitted that “a ratio of the total area of the Schottky structure to the total area of the MOSFET in the range of 2.5% to 5% results in optimum performance”. (See page 6, lines 24-26).

With respect to claim 14, the field effect transistor of Sapp further comprises a metal layer (216) contacting the pair of doped source regions (212), the metal layer (216) and the barrier layer (218) comprise one of either titanium tungsten or titanium nitride.

With respect to claim 15, the barrier layer (218) and the metal layer (216) contacting the source regions (212) connect together by an overlying layer of metal.

With respect to claim 16, the barrier layer (218) of Sapp forms the Schottky diode anode terminal and the substrate (202) forms the Schottky diode cathode terminal.

With respect to claim 17, in view of Baliga, the monolithically integrated structure of Sapp further includes: a second trench (200-1) adjacent to the first trench (200-2), the second trench including (as discussed above) a third conductive material (26) forming a shield electrode and a fourth conductive material (30) forming a gate electrode over but insulated from the third conductive material (26), wherein a distance between the first trench (200-2) and the second trench (200-1) is greater than a distance W separating the pair of adjacent trenches (200-3; 200-4), and wherein the barrier layer (218) and a metal layer (216) contacting the source regions (212) of the field effect transistor comprise one of either titanium tungsten or titanium nitride.

With respect to claim 18, in view of Baliga, the lower sidewalls (20a) and bottom (20b) of the first trench (20) is lined with a shield dielectric, and upper sidewalls (28) of the first trench (20) are lined with a gate dielectric, the shield dielectric (20a, 20b) being thicker than the gate dielectric (28).

***Response to Arguments***

6. Applicant's arguments filed May 3, 2007 have been fully considered but they are not persuasive.

**The Support for New Matter:**

Regarding the new percentage area of the Schottky, Applicant states: "Support for this amendment can be found in the specification".

However, the specification fails to explicitly support for 4.5%, nor shows any thing that is unexpected at 4.5%. The best answer Applicant have put forth in the interview conducted in May 3, 2007 were "4.5% is within the range of 2.5% to 5%.

Applicant must provide support for or cancel the new matter.

**Rejection under 35 U.S.C 103(a):**

Through out the argument, Applicant only directed to the range of 2.5% to 5%, instead of the claimed range of 2.5% to 4.5%.

Since the percentage area of the Schottky structure taught by Korman to include about 5%, thus, the combination of the references clearly renders the 2.5% to 5% obvious.

***Conclusion***

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Anh D. Mai/  
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